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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/650,445	08/28/2003	Chun-Chieh Lin	TSM02-1369	6733
43859	7590	12/16/2004	EXAMINER	
SLATER & MATSIL, L.L.P. 17950 PRESTON ROAD, SUITE 1000 DALLAS, TX 75252			NADAV, ORI	
			ART UNIT	PAPER NUMBER
			2811	

DATE MAILED: 12/16/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/650,445

Applicant(s)

LIN ET AL.

Examiner

ori nadav

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 21 October 2004.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-11 and 26-36 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-11 and 26-36 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-11 and 26-36 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The claimed limitations of a dielectric pedestal disposed within and integral to said layer of dielectric material located above remaining portions of said layer of dielectric material, as recited in claims 1 and 26, are unclear as to how a dielectric pedestal is disposed within a layer of dielectric material, which layer is located above remaining portions of said layer of dielectric material, and which are the remaining portions of said layer of dielectric material.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

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Claims 1-11, insofar as in compliance with 35 U.S.C. 112, are rejected under 35 U.S.C. 102(e) as being anticipated by Yu (6,420,218).

Yu teaches in figure 1 and related text an integrated circuit device, comprising: a semiconductor device, including:

- a layer of dielectric material overlying a substrate 14;

- a dielectric pedestal 17, 35 disposed within and integral to said layer of dielectric material located above remaining portions of said layer of dielectric material and having first sidewalls; a channel region 37 located above said dielectric pedestal and having second sidewalls; and

- source and drain semiconductor regions 22, 24 disposed adjacent said first sidewalls of said dielectric pedestal and partially overlying said remaining portions of the layer of dielectric material opposing said channel region and each substantially spanning one of said second sidewalls,

- wherein said first and second sidewalls are substantially coincident,

- wherein each of said source and drain regions further substantially spans one of said first sidewalls,

- wherein said dielectric pedestal and said substrate form at least a portion of a silicon-on-insulator (SOI) substrate,

- wherein said channel region, said dielectric pedestal and said substrate form at least a portion of a silicon-on-insulator (SOI) substrate,

- wherein said dielectric pedestal is at least a portion of a buried oxide (BOX) layer located in said substrate,

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wherein said semiconductor device includes a silicide layer 56 over at least portions of said source and drain regions,

wherein said semiconductor device includes a gate structure having a gate oxide 37 located above said channel region and a gate electrode 36 located above said gate oxide,

wherein said gate oxide has a thickness ranging between about 0.2 nm and about 2 nm,

wherein said channel region has a length ranging between about 2 nm and about 100 nm, and

wherein said channel region has a thickness ranging between about 1 nm and about 20 nm.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 26-36, insofar as in compliance with 35 U.S.C. 112, are rejected under 35 U.S.C. 103(a) as being unpatentable over Yu in view of Vu et al. (5,807,771).

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Yu teaches substantially the entire claimed structure, as applied to claims 1-11 above, and including an interlevel dielectric layer located over said semiconductor device (column 7, lines 39-40). Yu does not state that vias spanning said interlevel dielectric layer and contacting said source and drain regions.

Vu et al. Teach in figure 9 and related text an interlevel dielectric layer located over a semiconductor device and vias 76 spanning said interlevel dielectric layer and contacting source and drain regions.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to form an interlevel dielectric layer over the semiconductor device of Yu and vias spanning said interlevel dielectric layer and contacting the source and drain regions in order to operate the device in its intended use.

Response to Arguments

Applicant argues that Yu does not teach the claimed invention, because Yu's oxide island material is not "integral to" the dielectric layer and it is not "located above remaining portions of said dielectric layer" as recited in claims 1 and 26.

Yu's oxide island material is "integral to" the dielectric layer, because both layers 17 and 35 comprise oxide and are thus indistinguishable from each other. Furthermore, Yu's oxide island material is clearly located

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above the dielectric layer, and is thus located above "remaining portions" of said dielectric layer, as recited in claims 1 and 26.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

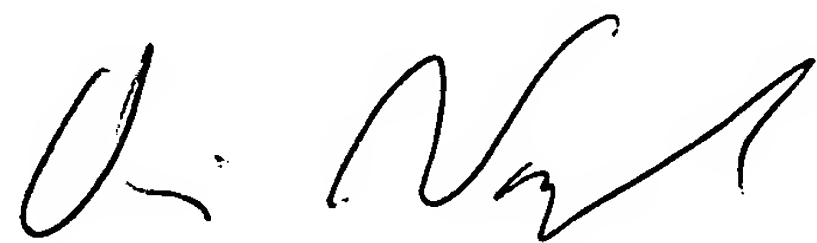
A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the date of this final action.

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Papers related to this application may be submitted to Technology center (TC) 2800 by facsimile transmission. Papers should be faxed to TC 2800 via the TC 2800 Fax center located in Crystal Plaza 4, room 4-C23. The faxing of such papers must conform with the notice published in the Official Gazette, 1096 OG 30 (November 15, 1989). The Group 2811 Fax Center number is (703) 308-7722 and 308-7724. The Group 2811 Fax Center is to be used only for papers related to Group 2811 applications.

Any inquiry concerning this communication or any earlier communication from the Examiner should be directed to *Examiner Nadav* whose telephone number is **(571) 272-1660**. The Examiner is in the Office generally between the hours of 7 AM to 4 PM (Eastern Standard Time) Monday through Friday.

Any inquiry of a general nature or relating to the status of this application should be directed to the **Technology Center Receptionists** whose telephone number is **308-0956**



O.N.
12/10/04

ORI NADAV
PRIMARY EXAMINER
TECHNOLOGY CENTER 2800